DS34C86T Quad CMOS Differential Line Receiver

Check for Samples: DS34C86T

FEATURES

- **CMOS Design for Low Power**
- **±0.2V Sensitivity Over the Input Common Mode Voltage Range**
- **Typical Propagation Delays: 19 ns**
- **Typical Input Hysteresis: 60 mV**
- **Inputs Won't Load Line when V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **TRI-STATE Outputs for System Bus Compatibility**
- **Available in Surface Mount**
- **Open Input Failsafe Feature, Output High for Open Input**

DESCRIPTION

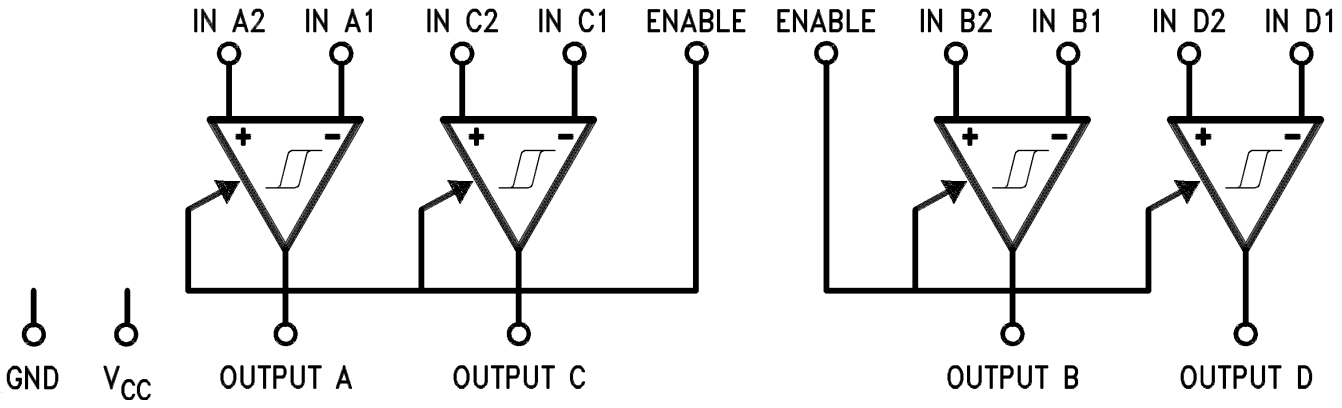
The DS34C86T is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86T has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34C86T features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE outputs have 6 mA source and sink capability. The DS34C86T is pin compatible with the DS3486.

Logic Diagram



Connection Diagram

Top View

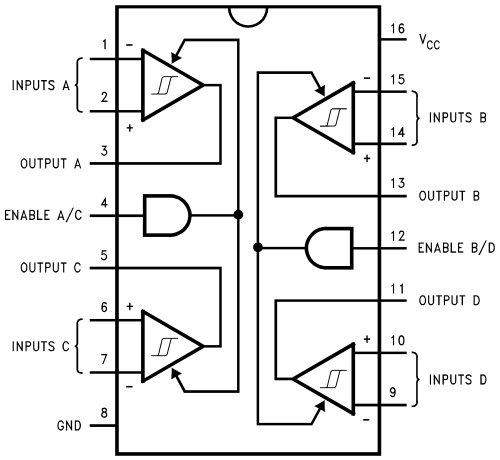


Figure 1. PDIP Package
See Package Numbers D0016A or NFG0016E

Truth Table(1)

Enable	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	H
H	$V_{ID} \leq V_{TH}$ (Min)	L
H	Open*	H

(1) Open, not terminated. Z = TRI-STATE

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)

Supply Voltage (V_{CC})	7V
Input Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C(5)	
PDIP Package	1645 mW
SOIC Package	1190 mW
Current Per Output	±25 mA
This device does not meet 2000V ESD rating(1)	

(1) ESD Rating; HBM (1.5kΩ, 100 pF) Inputs ≥ 2000V All other pins ≥ 1000V EIAJ (0Ω, 200 pF) ≥ 350V
(2) Unless otherwise specified, all voltages are referenced to ground.
(3) Absolute Maximum Ratings are values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The “Electrical Characteristics” provide conditions for actual device operation.
(4) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(5) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG0016E Package 13.16 mW/°C, and D0016A Package 9.52 mW/°C.

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics(1)

V_{CC} = 5V ±10% (unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	V_{OUT} = V_{OH} or V_{OL} −7V < V_{CM}< +7V	−200	35	+200	mV
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	5.0	6.8	10	kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +10V, Other Input = GND		+1.1	+1.5	mA
		V_{IN} = −10V, Other Input = GND		−2.0	−2.5	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)}$ = +1V I_{OUT} = −6.0 mA	3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)}$ = −1V I_{OUT} = 6.0 mA		0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	µA
I_I	Maximum Enable Input Current	V_{IN} = V_{CC} or GND			±1.0	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)}$ = +1V		16	23	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V		60		mV

(1) Unless otherwise specified, Min/Max limits apply across the operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

AC Electrical Characteristics(1)

V_{CC} = 5V ±10% (unless otherwise specified) (Figure 2, Figure 3, Figure 4)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		19	30	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	18	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	21	ns

(1) Unless otherwise specified, Min/Max limits apply across the operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Comparison Table of Switching Characteristics into "LS-Type" Load(1)

V_{CC} = 5V, T_A = 25°C (Figure 5, Figure 6)

Parameter		DS34C86		DS3486		Units
		Typ	Max	Typ	Max	
$t_{PHL(D)}$	Propagation Delay Time Output High to Low	17		19		ns
$t_{PLH(D)}$	Propagation Delay Time Output Low to High	19		19		ns
t_{PLZ}	Output Low to TRI-STATE	13		23		ns
t_{PHZ}	Output High to TRI-STATE	12		25		ns
t_{PZH}	Output TRI-STATE to High	13		18		ns
t_{PZL}	Output TRI-STATE to Low	13		20		ns

(1) This table is provided for comparison purposes only. The values in this table for the DS34C86 reflect the performance of the device but are not tested or specified.

TEST AND SWITCHING WAVEFORMS

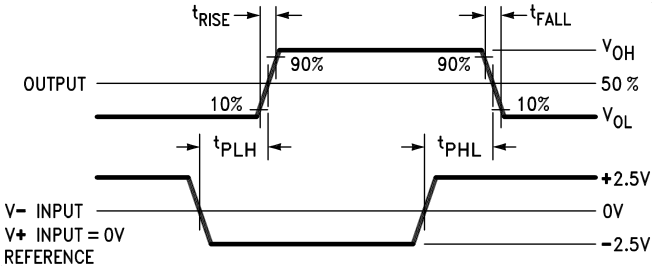
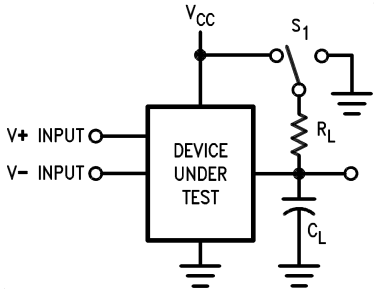


Figure 2. Propagation Delays



C_L Includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

Figure 3. Test Circuit for TRI-STATE Output Tests

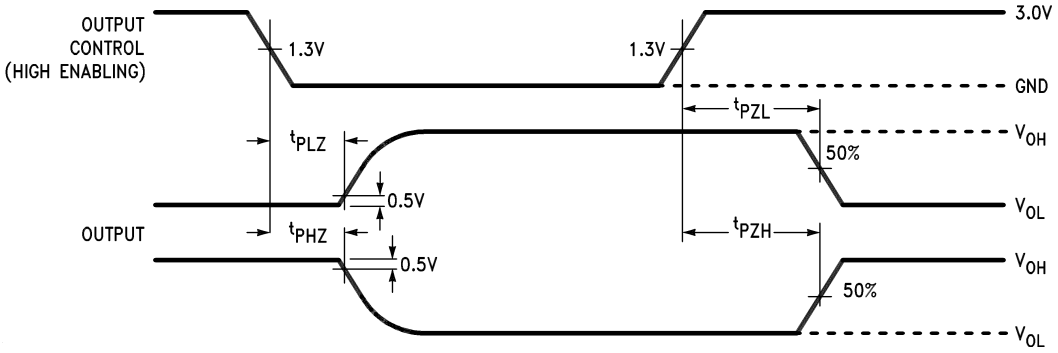
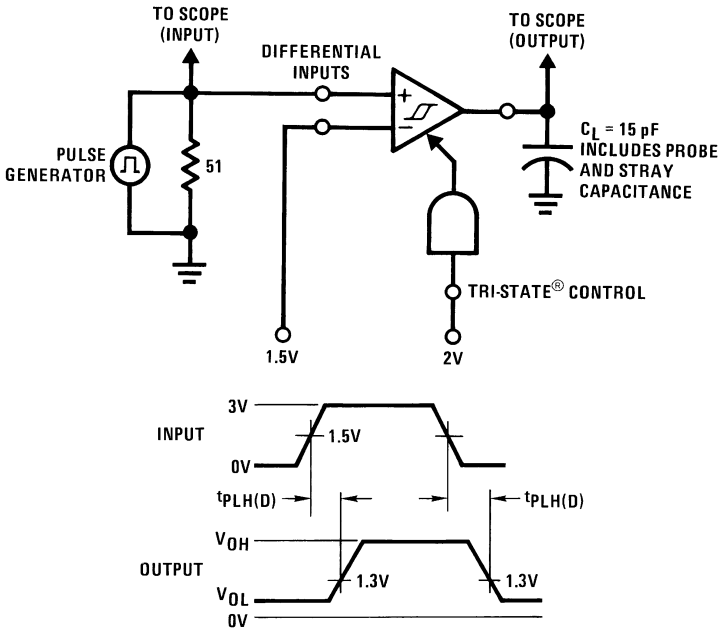


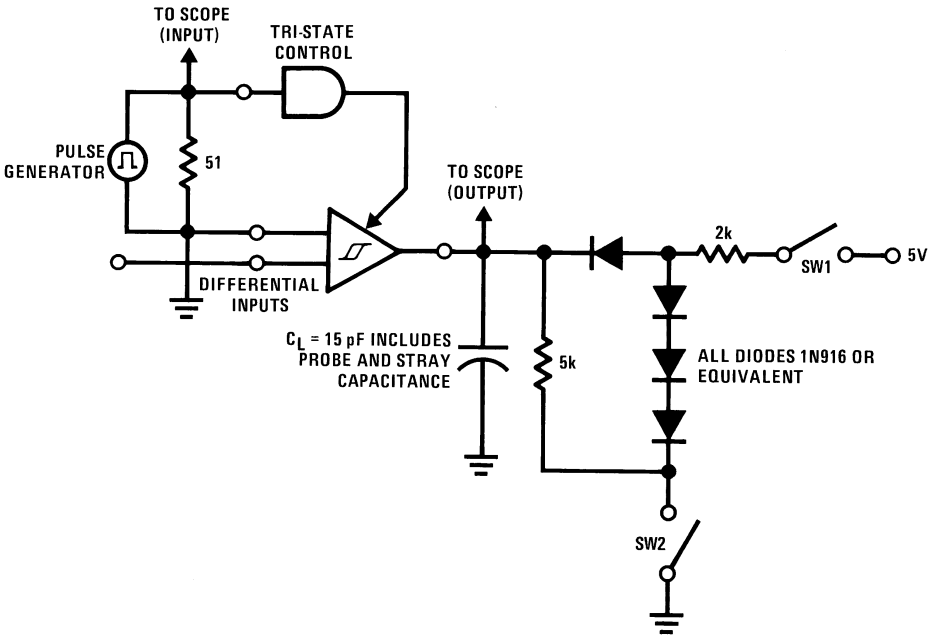
Figure 4. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuits and Switching Time Waveforms



Input Pulse Characteristics:
$t_{TLH} = t_{THL} = 6$ ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

Figure 5. Propagation Delay Differential Input to Output for "LS-Type" Load



1.5V for t_{PHZ} and t_{PLZ}
−1.5V for t_{PLZ} and t_{PZL}
Input Pulse Characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

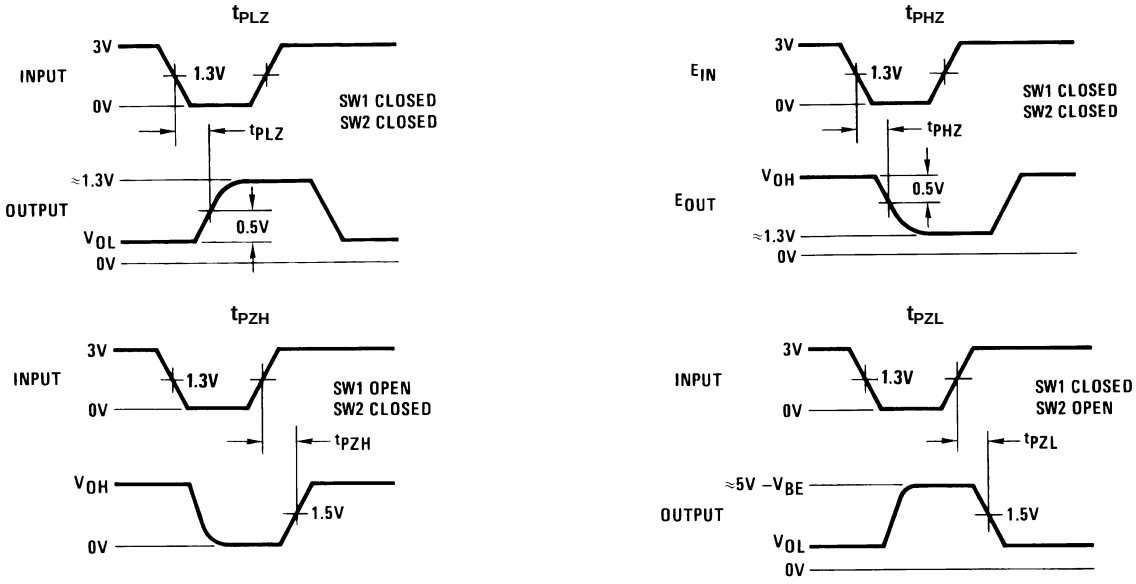


Figure 6. Propagation Delay TRI-STATE Control Unit to Output for “LS-Type” Load

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34C86TM/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS34C86TM	Samples
DS34C86TMX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS34C86TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

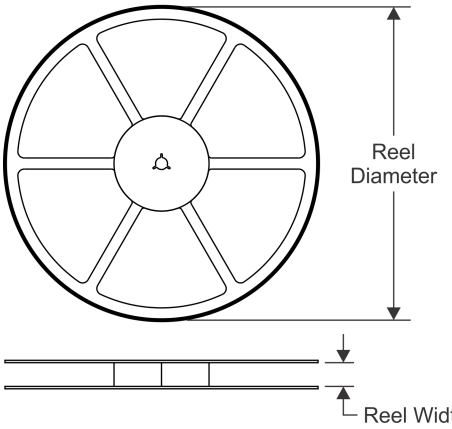
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

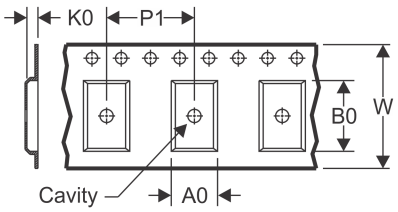
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

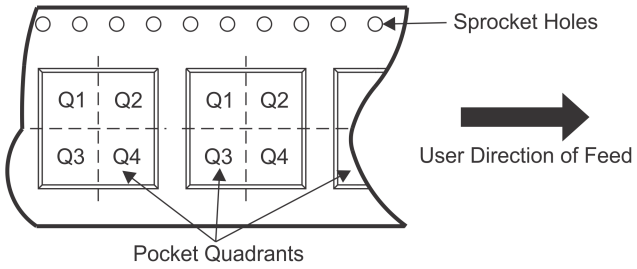


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

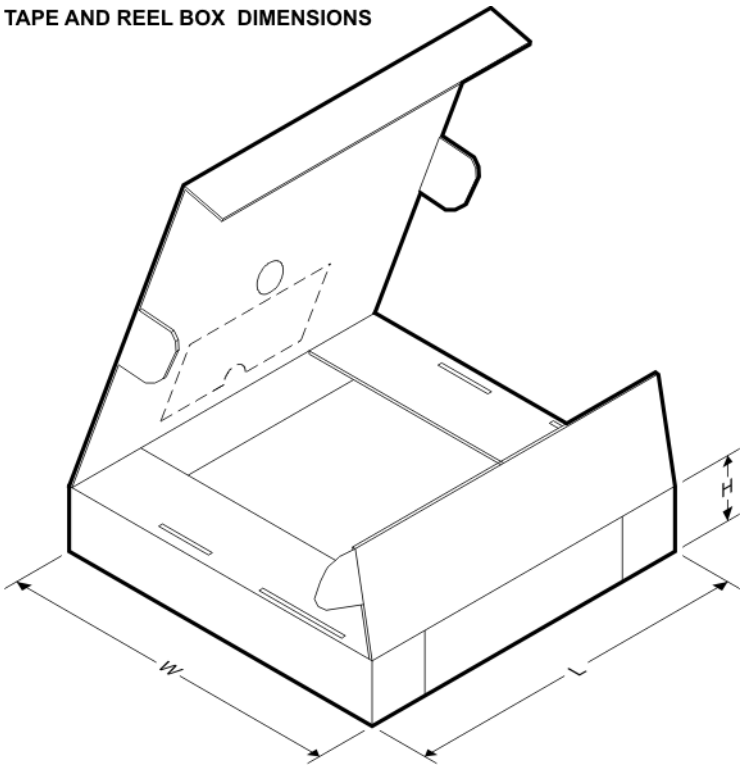
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34C86TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

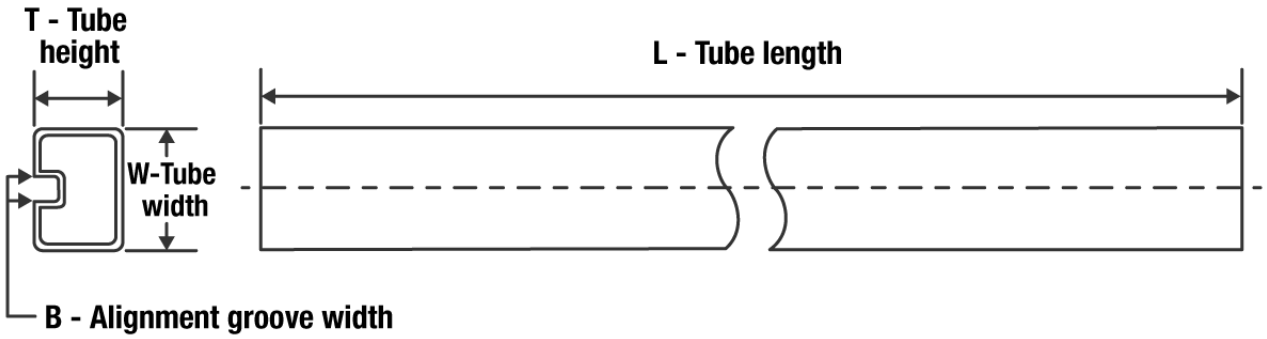
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34C86TMX/NOPB	SOIC	D	16	2500	356.0	356.0	35.0

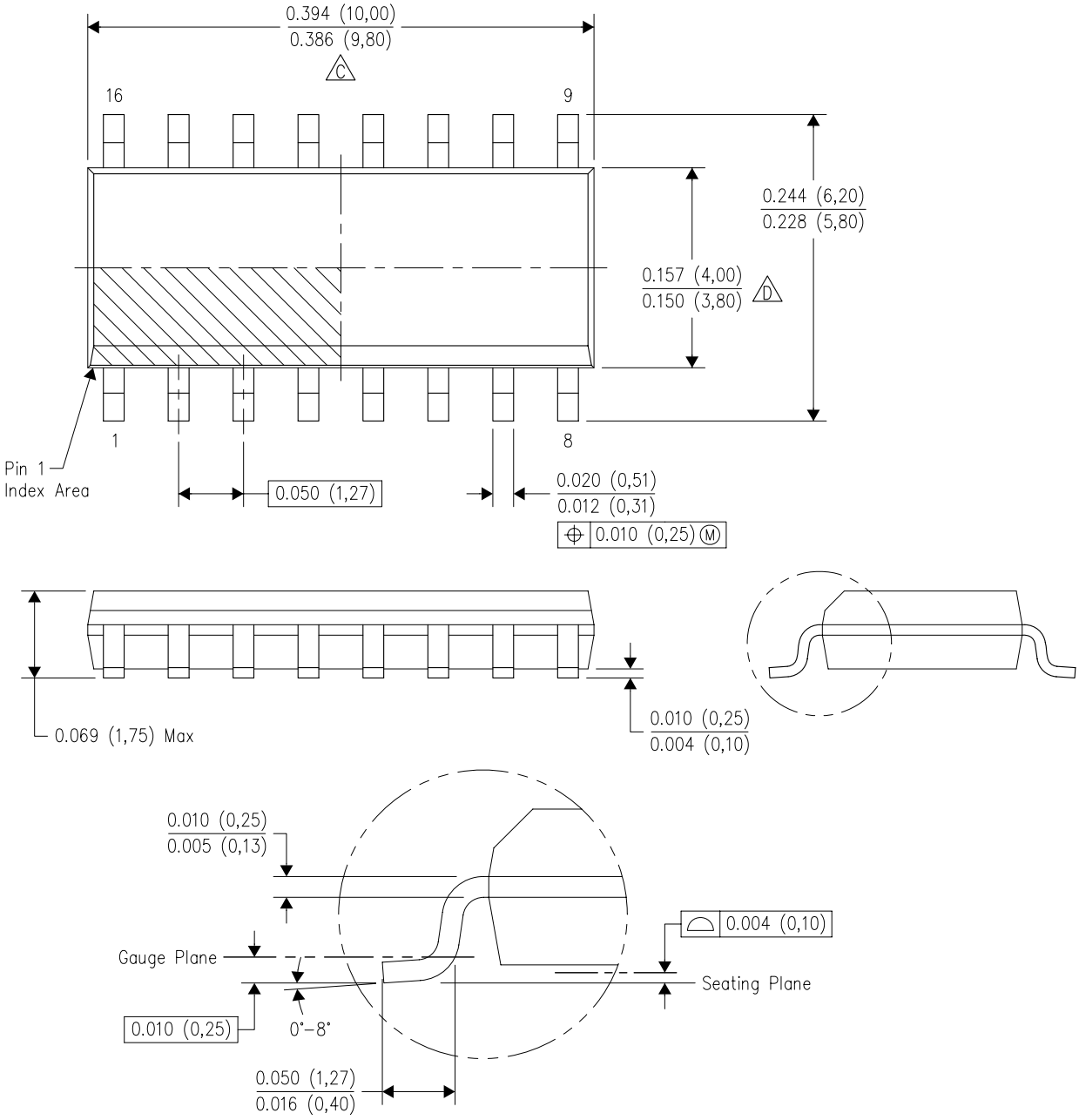
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS34C86TM/NOPB	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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